

BENJAMIN J. BLALOCK

7028 Rockingham Drive
Knoxville, TN 37909

Home: (865) 766-0746
Office: (865) 974-0927
Email: bblalock@ece.utk.edu
<http://www.ece.utk.edu/~bblalock>

EXPERIENCE:

The University of Tennessee, Knoxville, Tennessee Aug. 2001-present
Assistant Professor. Teaching emphasis on analog microelectronics.
Research focus on SOI analog/mixed-signal IC design, biomicroelectronics, development of CMOS analog/mixed-signal circuits for extreme environments, and design techniques for ultra low-voltage mixed-signal circuits.

Mississippi State University, Starkville, Mississippi Nov. 1996-Jul. 2001
Assistant Professor. Taught split-level (undergraduate and graduate) courses in digital VLSI and graduate courses in analog IC design. Conducted research and generated funding in CMOS VLSI mixed-signal IC design, low-voltage SOI and bulk-CMOS analog IC design, low-voltage/low-power CMOS digital IC design, SOI CMOS analog IC design for space applications, and Silicon-Carbide analog IC design. Affiliate faculty of the Engineering Research Center (ERC).

Mississippi State University, Starkville, Mississippi Aug. 2001-present
Adjunct Asst. Professor. Primary role is providing thesis direction.

Concorde Microsystems, Inc., Knoxville, Tennessee 1999-present
Analog/Mixed-Signal IC Design Consultant. Design work has included 8-bit MOSFET-only R-2R digital-to-analog converter and 5V precision bandgap voltage reference.

Cypress Semiconductor, Corp., Starkville, Mississippi 1999
Analog IC Design Consultant. Design work included a low-voltage comparator for multi-standard I/O.

Cypress Semiconductor, Corp., Starkville, Mississippi Summer 1997
Faculty Intern. Design of a voltage regulator and “zero-power” POR (power-on reset) circuit, both in CMOS SRAM technology

Georgia Institute of Technology, Atlanta, Georgia 1993-1996
Graduate Research Assistant, School of Electrical & Computer Engineering. Research focus included noise characterization of GaAs MESFETs, BiCMOS operational amplifier design, CMOS current-feedback amplifier design, and ultra low-voltage CMOS analog circuit

design for signal processing and power management applications.
Advisor: Dr. Phillip E. Allen

Computer Technology and Imaging, Inc., Knoxville, Tennessee Summer 1991
Research and Development Engineer. Design of 8-bit CMOS digital-to-analog converter using binary-weighted currents based on CMOS-compatible lateral BJTs.

University of Tennessee, Knoxville, Tennessee 1990-1991
Teaching Assistant for Electronics Laboratory, Department of Electrical and Computer Engineering. Assisted undergraduate students with electronics projects and was responsible for checking project performance specifications.

Hewlett Packard, Santa Clara, California Summer 1990
SEED (Student Educational Employment Development) Employee. Developed AC Test Hardware for testing bipolar integrated circuits at frequencies up to 3 GHz at the wafer level.

Cosmos, Inc., Santa Clara, California 1989-1990
Design Consultant. Developed medical applications firmware for R.W. Knierim, D.D.S.

EDUCATION:

Georgia Institute of Technology, Atlanta, Georgia 1993-1996
Doctor of Philosophy in Electrical and Computer Engineering.
Dissertation: "A 1-Volt CMOS Wide Dynamic Range Operational Amplifier." Advisor: Dr. Phillip E. Allen

Georgia Institute of Technology, Atlanta, Georgia 1991-1993
Master of Science in Electrical and Computer Engineering. Emphasis in analog and digital microelectronics.

University of Tennessee, Knoxville, Tennessee 1986-1991
Bachelor of Science in Electrical Engineering. Emphasis in electronics. Cooperative education student with Computer Technology and Imaging, Inc., Knoxville, Tennessee.

JOURNAL PAPERS:

B. Dufrene, K. Akarvardar, S. Cristoloveanu, B. J. Blalock, P. Gentil, E. Kolawa, M. M. Mojarradi, "Investigation of the Four Gate Action in G4-FETs," *IEEE Trans. on Electron Devices*, vol. 51, no. 11, pp. 1931-1935, Nov. 2004.

B.K. Swann, B.J. Blalock, L.G. Clonts, E. Breeding, M. Baldwin, J.M. Rochelle, and D.M. Binkley, "A 100 ps Time Resolution CMOS Time-to-Digital Converter for Positron Emission Tomography Imaging Applications," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 11, pp. 1839-1852, Nov. 2004.

B. Dufrene, B. Blalock, S. Cristoloveanu, K. Akarvardar, T. Higashino, and M. Mojarradi, "Subthreshold slope modulation in G^4 -FET transistors," *Microelectronic Engineering*, vol. 72, pp. 347-351, April 2004.

Ying Li, G. Niu, J.D. Cressler, J. Patel, M. Liu, M.M. Mojarradi, R.A. Reed, P.W. Marshall, B.J. Blalock, "Probing Proton Damage in SOI CMOS Technology by Using Lateral Bipolar Action," *IEEE Trans. on Nuclear Science*, vol. 50, no. 6, pp. 1885-1890, Dec. 2003.

S.C. Terry, J.M. Rochelle, D.M. Binkley, B.J. Blalock, and D. Foty, "Comparison of a BSIM3V3 and EKV MOST Model for a 0.5um CMOS Process and Implications for Analog Circuit Design," *IEEE Trans. on Nuclear Science*, vol. 50, no. 4, pp. 915-920, Aug. 2003.

B.K. Swann, J.M. Rochelle, D.M. Binkley, B.S. Puckett, S.C. Terry, B. J. Blalock, K.M. Baldwin, E. Breeding, M. Musrock, and J. Young, "A Custom Mixed Signal CMOS Integrated Circuit for High Performance PET Tomograph Front-End Applications," *IEEE Trans. on Nuclear Science*, vol. 50, no. 4, pp. 909-914, Aug. 2003.

M.N. Ericson, J.M. Rochelle, C.L. Britton, B.J. Blalock, A. Wintenberg, and D.M. Binkley, "Flicker Noise Behavior of MOSFETs Fabricated in 0.5-micron Fully-Depleted (FD) Silicon-on-Sapphire (SOS) CMOS In Weak, Moderate, and Strong Inversion," *IEEE Trans. on Nuclear Science*, vol. 50, no. 4, pp. 963-968, Aug. 2003.

Ying Li, Guofu Niua, John D. Cressler, Jagdish Patel, S.T. Liu, Robert A. Reed, Mohammad M. Mojarradi and Benjamin J. Blalock, "The Operation of 0.35 μ m Partially-Depleted SOI CMOS Technology in Extreme Environments," *Solid-State Electronics*, vol. 47, no. 6, pp. 1111-1115, June 2003.

Mohammad Mojarradi, David Binkley, Benjamin Blalock, Richard Andersen, Norbert Ulshoefer, Travis Johnson, Linda Del Castillo, "A Miniaturized Neuroprosthesis Suitable for Implantation into the Brain," *IEEE Trans. on Neural Systems and Rehabilitation Engineering*, vol. 11, no. 1, pp. 38-42, Mar. 2003.

Venkatesh Srinivasan, Syed K. Islam, and Benjamin J. Blalock, "Minimizing Phase Noise Variation in CMOS Ring Oscillators," *Analog Integrated Circuits and Signal Processing*, vol. 34, pp. 259-263, Mar. 2003.

B. J. Blalock, S. Cristoloveanu, B. M. Dufrene, F. Allibert, and M. M. Mojarradi, "The Multiple-Gate MOS-JFET Transistor," *Int. J. of High Speed Electronics and Systems*, vol. 12, no. 2, pp. 511-520, 2002.

S. A. Jackson, J. Killens, and B. J. Blalock, "A Programmable Current Mirror for Analog Trimming Using Single-Poly Floating Gate Devices in Standard CMOS Technology," *IEEE Trans. on Circuits and Systems II*, vol. 48, no. 1, pp. 100-102, Jan. 2001.

B. J. Blalock, P. E. Allen, and G. A. Rincon-Mora, "Designing 1-V Op Amps using Standard Digital CMOS Technology," *IEEE Trans. on Circuits and Systems II*, vol. 45, no. 7, pp. 769-780, July 1998.

REFEREED CONFERENCE PAPERS:

S.C. Terry, S. Chen, B.J. Blalock, J.R. Jackson, B.M. Dufrene, M.M. Mojarradi, S.K. Islam, and M.N. Ericson, "Temperature Compensated Reference Circuits for SOI," *2004 IEEE International SOI Conference*, Charleston, South Carolina, October 4-7, 2004.

S.C. Terry, B.J. Blalock, J.M. Rochelle, and M.N. Ericson, "Time-domain noise analysis of linear time-invariant and linear time-variant systems using MATLAB and HSPICE," accepted to the *2004 IEEE Nuclear Science Symposium*, Rome, Italy, October 16-22, 2004.

D. Binkley, J. Cressler, B. Blalock, and M. Mojarradi, "Noise Performance on 0.35- μ m SOI CMOS Devices and Micropower Preamplifier Following 63-MeV, 1-Mrad (Si) Proton Irradiation," *2004 IEEE Nuclear and Space Radiation Effects Conference*, Atlanta, Georgia, July 19-23, 2004.

K. Akarvardar, S. Cristoloveanu, B. Dufrene, B. Blalock, M. Mojarradi, and P. Gentil, "Low-Temperature Mechanisms and Properties of the SOI 4-Gate Transistor (G4-FET)," *Sixth European Workshop on Low Temperature Electronics (WOLTE-6)*, pp. 127-132, ESTEC, Noordwijk, The Netherlands, June 23-25, 2004.

S.C. Terry, B.J. Blalock, J.R. Jackson, S. Chen, C.S.A. Durisety, M.M. Mojarradi, and E.A. Kolawa, "Development of Robust Analog and Mixed-Signal Electronics for Extreme Environment Applications," *2004 IEEE Aerospace Conference*, Big Sky, Montana, March 7-12, 2004.

M.N. Ericson, M. Bobrek, A. Bobrek, C.L. Britton, J.M. Rochelle, B.J. Blalock, and R.L. Schultz, "A High Resolution, Extended Temperature Sigma Delta ADC in 3.3V 0.5 μ m SOS-CMOS," *2004 IEEE Aerospace Conference*, Big Sky, Montana, March 7-12, 2004.

M.M. Mojarradi, R.S. Cozy, Y. Chen, M. Johnson, E.A. Kolawa, M. Johnson, T. McCarthy, G.C. Levanas, B. Blalock, G. Burke, L. Del Castillo, and A.A. Shapiro, "Application of Commercial Electronics in the Motors and Actuator Systems for Mars Surface Missions," *2004 IEEE Aerospace Conference*, Big Sky, Montana, March 7-12, 2004.

D.M. Binkley, C.E. Hopper, B.J. Blalock, M.M. Mojarradi, J.D. Cressler, and L.K. Yong, "Noise Performance of 0.35- μm SOI CMOS Devices and Micropower Preamplifier from 77 – 400 K," *2004 IEEE Aerospace Conference*, Big Sky, Montana, March 7-12, 2004.

B. Dufrene, K. Akarvardar, S. Cristoloveanu, B. Blalock, P. Fechner, and M. Mojarradi, "The G4-FET: Low Voltage to High Voltage Operation and Performance," *Proc. of the 2003 IEEE Int. SOI Conf*, pp. 55-56, Newport Beach, California, September 29–October 2, 2003.

M.N. Ericson, C.L. Britton, J.M. Rochelle, B.J. Blalock, B.D. Williamson, R.L. Greenwell, and R. Schultz, "High Temperature DC Characterization of Fully-Depleted 0.5 μm SOS-CMOS MOSFETs For Analog Circuit Design," *Proc. of the 2003 IEEE Int. SOI Conf*, pp. 89-91, Newport Beach, California, September 29–October 2, 2003.

D.M. Binkley, D.H. Ihme, B.J. Blalock, and M.M. Mojarradi, "Micropower, 0.35- μm Partially Depleted SOI CMOS Preamplifiers having Low White and Flicker Noise," *Proc. of the 2003 IEEE Int. SOI Conf*, pp. 85-86, Newport Beach, California, September 29–October 2, 2003.

K. Akarvardar, B. Dufrene, S. Cristoloveanu, B.J. Blalock, T. Higashino, M.M. Mojarradi, and E. Kolawa, "Multi-Bias Dependence of Threshold Voltage, Subthreshold Swing, and Mobility in G4-FETs," *Proc. of the 2003 European Solid-State Device Research Conf. (ESSDERC)*, pp. 127–130, Estoril, Portugal, September 16–18, 2003.

B. Dufrene, B. Blalock, S. Cristoloveanu, K. Akarvardar, T. Higashino, and M. Mojarradi, "Subthreshold Slope Modulation in G4-FET Transistors," accepted to *INFOS '03*, June 2003.

S.C. Terry, B.J. Blalock, J.R. Jackson, S. Chen, M.M. Mojarradi, and E.A. Kolawa, "Development of Robust Analog Electronics at the University of Tennessee for NASA/JPL Extreme Environment Applications," **invited paper** in the *2003 Proc. of the University/Government/Industry Microelectronics Symp.*, pp. 124-127, Boise, Idaho, June 30-July 2, 2003.

D.M. Binkley, D.H. Ihme, C.E. Hopper, B.J. Blalock, and M.M. Mojarradi, "Micropower, Low-Noise, SOI CMOS Preamplifiers for Deep Space Missions," *2003*

Proc. of the University/Government/Industry Microelectronics Symp., pp. 112-115, Boise, Idaho, June 30-July 2, 2003.

B. Dufrene, B. Blalock, S. Cristoloveanu, M. Mojarradi, and E.A. Kolawa, "Saturation Current Model for the N-channel G^4 -FET," *2003 Proc. of the Electrochemical Society*, vol. 2003-05, pp.367-372, Paris, France, April 27-May 2, 2003.

Y. Li, G. Niu, J.D. Cressler, J. Patel, M. Liu, R. Reed, M.M. Mojarradi, and B.J. Blalock, "Operating SOI CMOS Technology in Extreme Environments," *Dig. of the 2003 IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, pp. 37-40, Munich, Germany, April 2003.

S.C. Terry, J.M. Rochelle, D.M. Binkley, B.J. Blalock, and D. Foty, "Comparison of a BSIM3V3 and EKV MOST Model for a 0.5um CMOS Process and Implications for Analog Circuit Design," *Conf. Record 2002 IEEE Nuclear Science Symp. and Medical Imaging Conf.*, Norfolk, VA, 2002.

B.K. Swann, J.M. Rochelle, D. M. Binkley, B.S. Puckett, S.C. Terry, B. J. Blalock, K.M. Baldwin, E. Breeding, M. Musrock, and J. Young, "A Custom Mixed Signal CMOS Integrated Circuit for High Performance PET Tomograph Front-End Applications," *Conf. Record 2002 IEEE Nuclear Science Symp. and Medical Imaging Conf.*, Norfolk, VA, 2002.

M.N. Ericson, J.M. Rochelle, C.L. Britton, B.J. Blalock, A. Wintenberg, and D.M. Binkley, "Noise Behavior of MOSFETs Fabricated in 0.5-micron Fully-Depleted (FD) Silicon-on-Sapphire (SOS) CMOS In Weak, Moderate, and Strong Inversion," *Conf. Record 2002 IEEE Nuclear Science Symp. and Medical Imaging Conf.*, Norfolk, VA, 2002.

S. Terry, B. J. Blalock, LK. Yong, B. Dufrene, and M. Mojarradi, "Complementary Body Driving – A Low Voltage Analog Circuit Technique for SOI," *Proc. of the 2002 IEEE Int. SOI Conf.*, pp. 80-82, Williamsburg, Virginia, October 2002.

M.N. Ericson, J.M. Rochelle, M. Bobrek, C.L. Britton, A. Bobrek, B. J. Blalock, R. Schultz, and J.A. Moore, "2nd- and 4th-Order $\Sigma\Delta$ Modulators Fabricated in 3.3V 0.5 μ m SOS-CMOS for High-Temperature Applications," *Proc. of the 2002 IEEE Int. SOI Conf.*, pp. 75-77, Williamsburg, Virginia, October 2002.

B.J. Blalock, S. Terry, B. Dufrene, C. Durisety, LK. Yong, S. Cristoloveanu, and M. Mojarradi, "An Overview of Circuits & Devices Research on SOI for Analog/Mixed-Signal Systems," **invited paper**, *Proc. of the 2002 IEEE Midwest Symp. Circuits & Syst.*, pp. 359-362, Tulsa, Oklahoma, August 2002.

J.W. Bruce, J.E. Creekmore, S.R. Porter, R.P. King, and B.J. Blalock, "Adaptive Design Method for Efficient Direct Digital Synthesis," *Proc. 2002 IEEE Midwest Symp. Circuits & Syst.*, pp. 545-548, Tulsa, Oklahoma, August 2002.

S. Cristoloveanu, B. Blalock, F. Allibert, B. M. Dufrene, and M. M. Mojarradi, "The Four-Gate Transistor," *Proc. of the 2002 European Solid-State Device Research Conf*, pp. 323-326, Firenze, Italy, September 2002.

M. C. D. Smith, J. B. Casady, P.B. Shah, B. Dufrene, B. Blalock, and S. E. Sadow "Dual-Gate 4H-SiC JFET Development," *Proc. of the International Conference on Silicon Carbide and Related Materials 2001*, Tsukuba, Japan, November 2001.

J.A. Bell, J.W. Bruce, B.J. Blalock, and P. Stubberud, "CMOS current mode flash analog to digital converter," *Proc. 2001 IEEE Midwest Symp. Circuits & Syst.*, pp. 272-275, Dayton, Ohio, August 2001.

J.E. Creekmore, S.R. Porter, J.W. Bruce, and B.J. Blalock, "Direct digital frequency synthesis using nonlinear digital-to-analog conversion," *Proc. 2001 IEEE Midwest Symp. Circuits & Syst.*, pp. 897-900, Dayton, Ohio, August 2001.

B. J. Blalock, H. W. Li, P. E. Allen, and S. A. Jackson, "Body-Driving as a Low-Voltage Analog Design Technique for CMOS Technology," invited paper in the *Proc. 2000 Southwest Symp. on Mixed-Signal Design*, 2000, pp. 113-118.

S. A. Jackson and B. J. Blalock, "An Active Substrate Driver for Mixed-Voltage SOI Systems On A Chip," in *Proc. 2000 Southwest Symp. on Mixed-Signal Design*, 2000, pp. 83-86.

B. J. Blalock and S. A. Jackson, "A 1.2-V CMOS Four-Quadrant Analog Multiplier," in *Proc. 1999 Southwest Symp. on Mixed-Signal Design*, 1999, pp. 1-4.

M. M. Mojarradi, E. Brandon, U. Lieneweg, R. Bugga, E. Wesseling, H. Li, and B. Blalock, "Power Management and Distribution for Systems on a Chip Applications," *AIAA Conference*, Paper 284, Albuquerque, New Mexico, Sept. 27-30, 1999.

S. A. Jackson and B. J. Blalock, "A CMOS Mixed-Signal Simultaneous Bidirectional Signaling I/O," in *Proc. 1998 IEEE Midwest. Symp. Circuits Syst*, 1998, pp. 37-40.

B. J. Blalock and P. E. Allen, "A One-Volt, 120- μ W, 1-MHz OTA for Standard CMOS Technology," in *Proc. 1996 IEEE Int. Symp. Circuits Syst*, 1996, pp. 305-307.

B. J. Blalock and P. E. Allen, "A Low-Voltage, Bulk-Driven MOSFET Current Mirror for CMOS Technology," in *Proc. 1995 IEEE Int. Symp. Circuits Syst*, 1995, pp. 1972-1975.

P. E. Allen, B. J. Blalock, and G. A. Rincon, "A 1-Volt CMOS Op Amp Using Bulk-Driven MOSFETs," in *Dig. 1995 IEEE Int. Solid-State Circuits Conf.*, Feb. 1995, pp.

192-193.

P. E. Allen, B. J. Blalock and G. A. Rincon, "Low-Voltage Analog Circuits Using Standard CMOS Technology," *Proc. 1995 IEEE Int. Symp. Low Power Design*, 1995, pp. 209-214.

P. E. Allen and B. J. Blalock, "The Influence of Device Selection on the Performance of a Simple BiCMOS Operational Amplifier," in *Proc. 1992 IEEE Midwest Symp. Circuits & Syst.*, 1992, pp. 912-915.

OTHER PUBLICATIONS:

B. J. Blalock, "A 1-Volt CMOS Wide Dynamic Range Operational Amplifier," (Ph.D. Dissertation, School of ECE, Georgia Institute of Technology, Atlanta, GA, 1996), © June 5, 1997.

P. E. Allen, B. J. Blalock, and S. W. Milam, "Active filters using low-gain amplifiers," in *The Circuits and Filters Handbook*, CRC press, Inc., 1995.

INVENTION DISCLOSURES:

"A radiation adaptive backgate driver circuit enabling higher voltage operation for SOI CMOS," M. M. Mojarradi, M. Underwood, B. Blalock, H. Li, April 1999, JPL/NASA case number NPO-20910.

"Complementary accumulation-mode JFET integrated circuit topology using wide (greater than 2eV) bandgap semiconductors," J. Casady, M. Mazzola, S. Sadow, B. Blalock, November 2001, Mississippi State University, Disclosure No. 0008018.

RESEARCH GRANTS AND CONTRACTS:

NASA/Jet Propulsion Laboratories, "Extreme Environment CMOS Mixed-Signal IC Design & Development for the Mars Science Laboratory - Phase II," *Principal Investigator*, \$74,902 (February 1, 2004 – January 31, 2005).

NASA/Jet Propulsion Laboratories, "G⁴-FET Based Memory," *Principal Investigator*, \$34,980 (January 1, 2004 – May 31, 2004).

The Boeing Company, "ADC Development on the SOI6 Process for the VDSM Program," *Principal Investigator*, \$67,253 (June 1, 2003 – May 31, 2004).

NASA/Jet Propulsion Laboratories, "Investigation of G⁴-FET Quantum Wire Properties & Applications," *Principal Investigator*, \$29,896 (June 1, 2003 – Sept. 30, 2003).

NASA/Jet Propulsion Laboratories, “Extreme Environment CMOS Mixed-Signal IC Design & Development for the Mars Science Laboratory,” *Principal Investigator*, \$9,995 (Mar. 1, 2003 – Oct. 31, 2003).

NASA/Jet Propulsion Laboratories, “SOI Analog Circuits & Devices for a Thin-Film Lithium-Ion Micro-Battery Charger System,” *Principal Investigator*, \$125,023 (Aug. 1, 2001 – Oct. 31, 2003).

DARPA, “Digital Electrostatic E-Beam Array Lithography, Metrology, and Inspection” (with C.E. Thomas, L.R. Baylor, D.H. Lowndes, G. Eres, D.B. Geohegan, V. Merkulov, A. Puretzky, M.L. Simpson, J.E. Hardy, J.A. Moore, J.B. Wilgen, M. Guillorn, J.H. Whealton, and E. Voelkl-Oak Ridge National Laboratory), \$3.5M (August 2001 – December 2003), *Co-PI* of Task 3 – “On-Chip Digitally Addressable Field-Emission Array,” \$416,450.

The Boeing Company, “Low-Voltage Analog IC Design in SOI technology for Very-Deep Sub-micron Systems-On-A-Chip,” *Principal Investigator*, \$88,230 (April 1, 2002 – March 31, 2003).

NASA/Jet Propulsion Laboratories, “Analog/Mixed-Signal Circuit Design and Evaluation to support Micro-Propulsion Systems,” *Principal Investigator*, \$28,000 (May 1, 2002 – February 28, 2003), conducted at The University of Tennessee.

NASA/Jet Propulsion Laboratories, “Analog/Mixed-Signal Circuit Design and Evaluation to support Micro-Propulsion Systems,” *Principal Investigator*, \$52,359 (March 1, 2000 – February 28, 2002), conducted at Mississippi State University.

NASA/Jet Propulsion Laboratories, “Analog/Mixed-Signal Circuit Design and Evaluation to support Power Systems for Mixed-Voltage Systems-On-A-Chip in SOI CMOS Technology,” *Principal Investigator*, \$60,158 for 1 year (2000).

NASA/Jet Propulsion Laboratories, “A Look-Up Table Based ADC with Continuous-Time Calibration,” *Principal Investigator*, \$24,549 for 3 months (2000).

Air Force/PERDA, “Development of Pilot Production Capabilities for Silicon Carbide Power Devices and Integrated Circuits,” *Co-PI*, \$1,609,261 for 15 months (2000-2001).

NASA/Jet Propulsion Laboratories, “Investigation of Analog Circuits and Techniques to support Power Systems for Systems-On-A-Chip in SOI CMOS Technology,” *Principal Investigator*, \$39,900 for 1 year (1999).

Boeing Military Aircraft & Missile Systems, “X2000 Design Services,” *Principal Investigator*, \$69,232 for 4.5 months (1999-2000).

National Security Agency, “Innovative PROM Circuits on a Bulk CMOS Line,”

Principal Investigator, \$28,000 for 1 year (1999).

Cypress Semiconductor, Corp., \$25,000 **annual** grant to support undergraduate & graduate research assistants within the Microsystems Prototyping Laboratory (now part of the Information Sensing Systems Laboratory) while at Mississippi State University (Initiated approximately 7 years ago by Dr. Trotter; since 1997, has been maintained by both BJB and Dr. Reese).

Cadence Design Systems, \$5,000 **annual** grant to support analog/mixed-signal IC design research (1999-2000).

Southeastern Center for Electrical Engineering Education (SCEEE) Research Initiation Grant, "Development of a 1-Volt Phaselocked Loop in Standard Digital CMOS Technology in MPL," *Principal Investigator*, \$10,000 for 1 year (1998).

NASA/Johnson Space Center, "Precision Operational Amplifier Design in 0.5-micron CMOS Technology," *Principal Investigator*, \$19,900 for 6 months (1998).

COURSES TAUGHT

While at MSU:

<u>Course No.</u>	<u>Title</u>
ECE 4263/6263	Introduction to VLSI Design (255 students to date)
ECE 8223	Analog IC Design (54 students to date)

Also 18 different Directed Studies covering miscellaneous topics related to digital, analog, or mixed-signal IC design and applications.

While at UT-Knoxville:

<u>Course No.</u>	<u>Title</u>
ECE 431/599	Operational Amplifier Circuits: Theory & Applications
ECE 432/599	Electronic Feedback Amplifiers
ECE 532	Analog IC Design II
ECE 335	Electronics I

AWARDS:

- Eta Kappa Nu *Outstanding Teacher* Award, Dept. of ECE, UT, April 2002
- *Cypress Semiconductor/MSU Industrial Fellow*, May 2001
- *DuPont Fellowship* recipient, 1991-1995
- *Eastman Kodak Scholarship* recipient, 1987-1991
- *Certificate of Appreciation from MSU/IMAGE* (an organization promoting educational opportunities for minorities), December 1999 & May 2000

PROFESSIONAL SERVICE:

Reviewer for:

IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications

IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing

IEEE Transactions on VLSI Systems

IEEE Transactions of Education

IEEE Transactions on Nuclear Science

IEE Proceedings – Circuits, Devices, and Systems

IEE Electronic Letters

2000 Southwest Symposium Mixed-Signal Design

2003 Southwest Symposium Mixed-Signal Design

2003 IEEE International Symposium on Circuits and Systems

Solid-State Electronics

NSF Review Panelist for “XYZ – Systems on a Chip” program

Program Committee, Southwest Symposium for Mixed-Signal Design, 2000 & 2003

Technical Program Committee, IEEE 15th University/Government/Industry Microelectronics Symposium (UGIM), 2003

Co-Chair of SOI Mixed-Signal Circuits Session & CMOS Mixed-Signal Circuits Session, IEEE UGIM Symposium, 2003

Member of:

IEEE Solid-State Circuits Society

IEEE Society of Circuits and Systems

IEEE Electron Devices Society

Eta Kappa Nu

Tau Beta Pi

Phi Kappa Phi

Committee Assignments

Mississippi State University:

ABET Committee (ad hoc), 1999-2000

Microelectronics Emphasis Committee, 1997-2001 (1999-2000 chairman)

Electronics Specialty Committee, 1997-2001

Lab Committee, 1998-2001

The University of Tennessee:

Electronics Search Committee Chairman, 2003

Nanotechnology/Devices Search Committee, 2001-2002

Graduate Committee, 2002-present

EXTERNAL COLLABORATORS:

David Binkley, Dept. of Elec. & Comp. Engr., Univ. of N. Carolina–Charlotte

John Cressler, School of Elec. & Comp. Engr., Georgia Tech

Sorin Cristoloveanu, LPCS/INPG, ENSERG, Grenoble, France

Herb Hess, Dept. of Elec. Engr., Univ. of Idaho

Bill Kuhn, Dept. of Elec. Engr., Kansas State Univ.

Harry Li, Dept. of Elec. Engr., Univ. of Idaho

Alan Mantooth, Dept. of Elec. Engr., Univ. of Arkansas

RESEARCH STUDENTS (listed by chronological order of graduation date):

Muhammad Addnan Islam, project student, "Low-Voltage Digital Design Techniques," MSCE, December 1997.

Yan Wang, project student, "1-V Static CMOS Logic Circuit Design in Standard CMOS Technology," MSEE, December 1997.

Srinivas Satish Bamdhamravuri, project student, "1-V Phase-Locked Loop in Standard CMOS Technology," MSEE, May 1998.

Jyothi Emmanuel Peddi, project student, "1-V Static CMOS Cell Library Development in Standard CMOS Technology," MSEE, May 1998.

Buddhika Abesingha, undergraduate research student focused on a 1-V VCO in Standard CMOS Technology, BSEE, August 1998.

Shohan Hossain, "Survey of ESD Structures for Sub-micron CMOS Technology," MSEE, December 1998.

Kailashnath Nagarakanti, project student, "Characterization of Single-Poly EEPROM Structures in Standard CMOS Technology," MSCE, December 1998.

Wei Qian, project student, "Design of a Low-Power Analog Multiplier," MSEE, December 1998.

Jinsong Zhao, project student, "Design of a CMOS VCO-DAC," MSEE, December 1998.

Chee-Leong Loh, thesis student, "Analog IC Design for Silicon Carbide Technology," MSEE, December 1999.

Yu Luan, project student, "CMOS Low-Voltage Constant-Gm Rail-to-Rail Input Range Op Amps," MSEE, December 1999.

Rangarajan Sanjay, project student, "Design of a 1-V DPLL in Standard CMOS Technology," MSCE, December 1999.

Jeremy Veldman, thesis student, "Analysis of the performance of an analog voltage comparator in SOI-CMOS versus Bulk-CMOS," MSEE, December 1999.

Scott Jackson, thesis student, “An Active Substrate Driver for Enabling Mixed-Voltage SOI Systems-On-A-Chip,” MSEE, May 2000; BSCE, December 1998.

Priyadarsini Erra, project student, “Design of a Latch Type Comparator in SOI Technology,” MSCE, May 2000.

Sooseok Oh, thesis student, “Design of a Compact Low-Voltage Rail-to-Rail Output Class-AB Op Amp in Fully-Depleted SOI Technology,” MSEE, August 2000.

Wai-tat Wong, thesis student, “Bandgap Voltage Reference Circuit in Partially-Depleted Silicon-On-Insulator CMOS Technology,” MSEE, August 2000.

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